Data Sheet July 1999 File Number 4611.1

Radiation Hardened Octal Non-Inverting Bidirectional Bus Transceiver

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD Total Dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil ACTS245T is a Radiation Hardened Octal Non-Inverting Bidirectional Bus Transceiver intended for two-way asynchronous communication between data busses.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ACTS245T are contained in SMD 5962-96719. A "hot-link" is provided from our website for downloading**.**
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9671901TRC	ACTS245DTR	-55 to 125
5962R9671901TXC	ACTS245KTR	-55 to 125

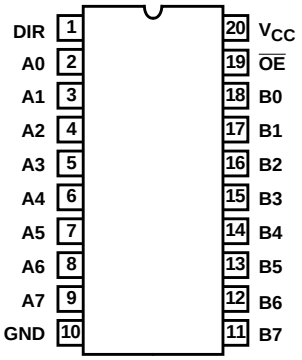
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

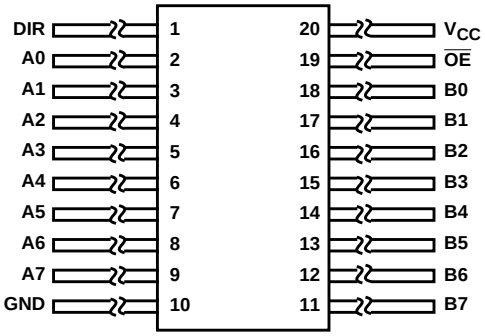
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - Latch-Up Free Under Any Conditions
  - Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
  - SEU LET Threshold . . . . . .>100 MEV-cm^2/mg
- 1.25 Micron Radiation Hardened SOS CMOS
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range. . . . . 4.5V to 5.5V
- Input Logic Levels
  - V_{IL} = 0.8V Max
  - V_{IH} = $V_{CC/2}$ Min
- Fast Propagation Delay . . . . . 18ns (Max), 12ns (Typ)

Pinouts

ACTS245T (SBDIP), CDIP2-T20
TOP VIEW

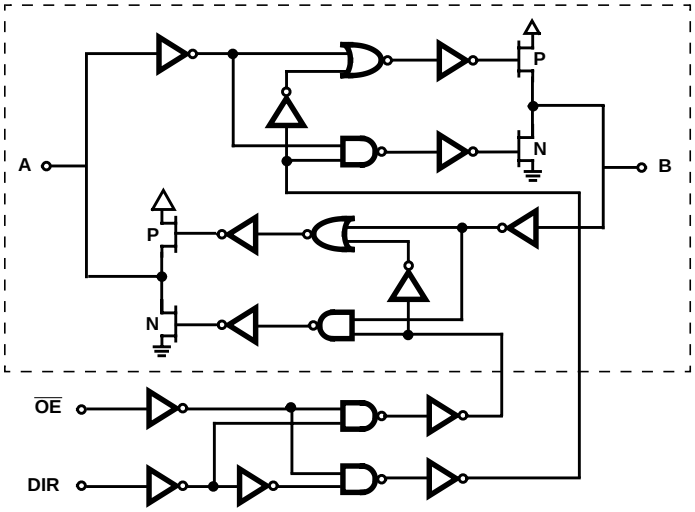


ACTS245T (FLATPACK), CDFP4-F20
TOP VIEW



Functional Diagram

NOTE: (1 of 8)



TRUTH TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

NOTE:

H = High Voltage Level, L = Low Voltage Level, X = Immaterial.

Die Characteristics

DIE DIMENSIONS:

(2440µm x 2970µm x 533µm ±51µm)

96 x 117 x 21mils ±2mil

METALLIZATION:

Type: Al Si Cu

Thickness: 10.0kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)

Bond Pad #20 (V_{CC}) First

Bond Pad #20 (V_{CC}) Uses Two Bond Wires

Bond Pad #10 (GND) Uses Two Bond Wires

BACKSIDE FINISH:

Sapphire

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8.0kÅ ±1.0kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

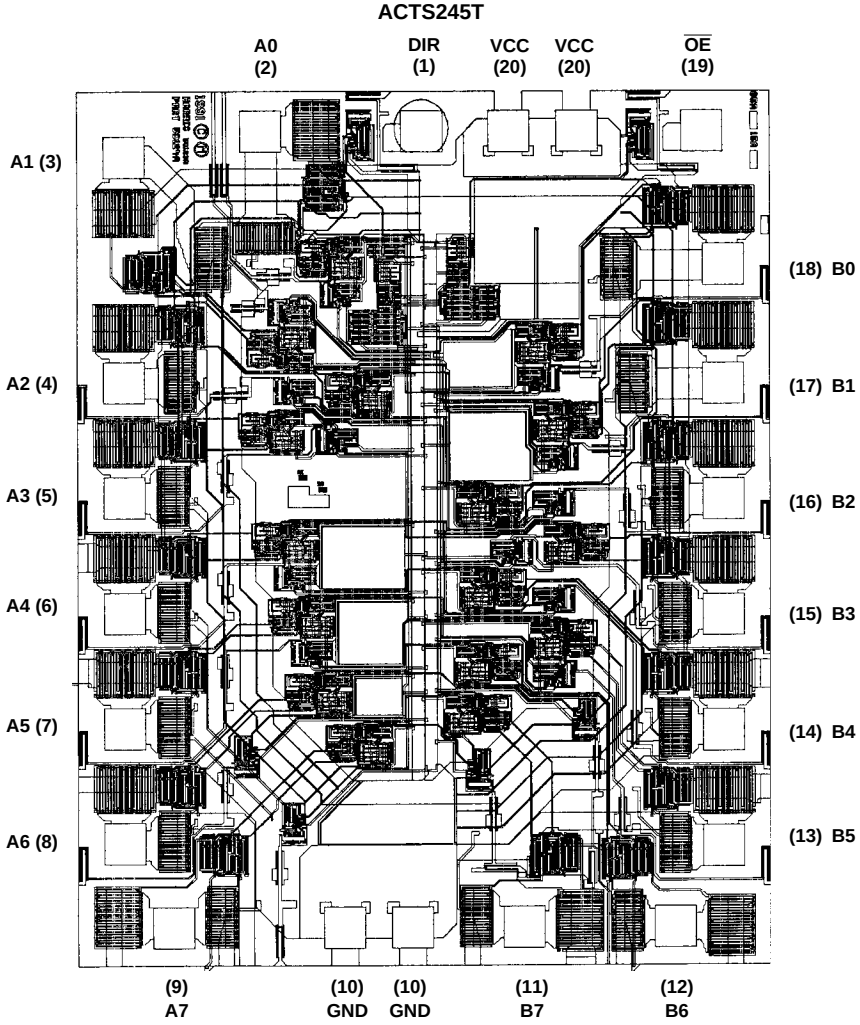
TRANSISTOR COUNT:

420

PROCESS:

CMOS SOS

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.